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Next generation of electronic systems: Challenges and solutions for microelectronic packaging

Rolf Aschenbrenner






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Outline

Microelectronic Packaging: Situation Analysis

Microelectronic Packaging DNA

Driving Factors, Examples

Wafer Level- and Panel Level Packaging

History

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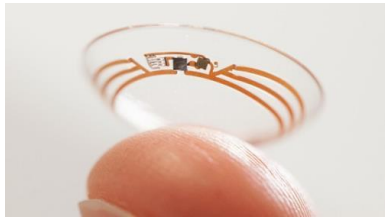
Microelectronic Packaging: Situation Analysis

Market Changes

- Consumer wants more & more functionality – MEMs, Sensors & more.
- Product Cost expectations are given
- Smart Phone superseded PC as the Market Driver
- Dynamic consumer business = new players dominating



With the mobile and smart phone era, the packaging industry is experiencing a flowering of new packages and reinvention of traditional packages.

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Re-inventing Packaging DNA

History

- For 40+ years, basic packaging DNA has been Au wirebond & Flip Chip
- Au wire bond was the interconnect work horse for the industry
- QFP, BGA and QFN were major innovations
- Flip Chip BGA on ceramic and on organic substrates have been the package of choice for PC MPU & GPU.

In last couple years, we have introduced new DNA:

- Cu Wirebond
- Flip Chip Cu Pillar
- Wafer level Packaging: WLCSP + WL fanout
- Embedded technologies
- 2.5 D Interposer – TXV
- 3D Packaging
- Heterogeneous integration

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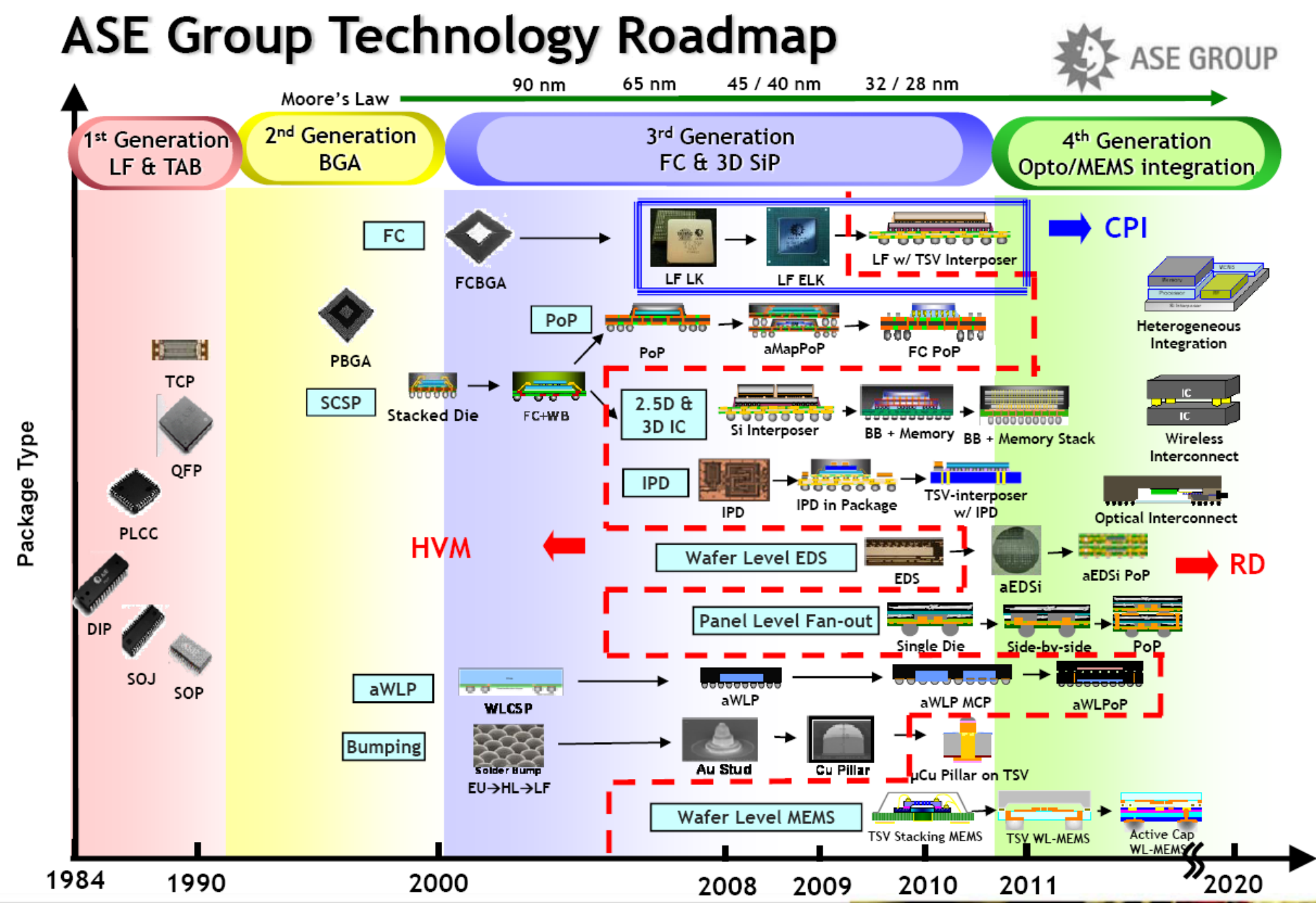
ASE Group Technology Roadmap



Ref.: Jisso & ASE

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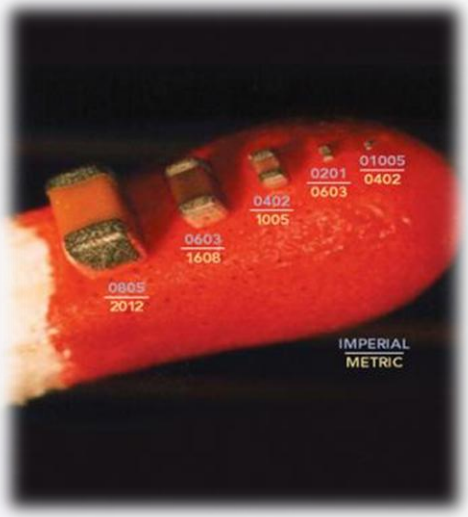
„THIN AND SMALL IS IN“



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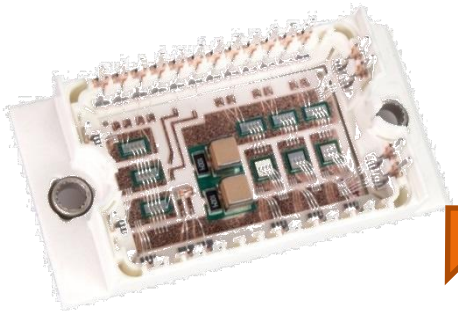
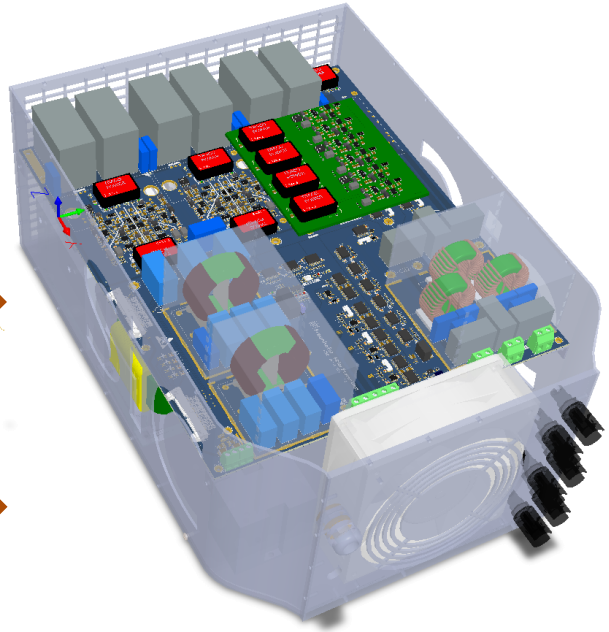
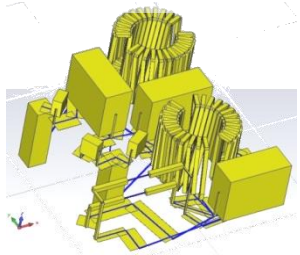
Example: Development of highly efficient SiC-Solar inverter

Packaging of Modules



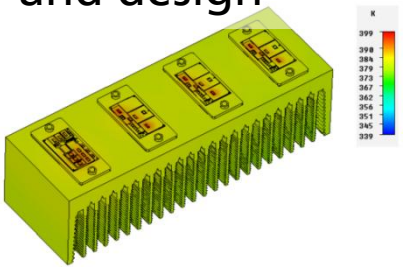


Mechanical and electrical design with EMC



Optimization of power loss

Thermal simulation and design



State of the art:
Si, 16 kHz, 45 kg

IZM Gen1:
SiC, 48 kHz, 15 kg

IZM Gen 2:
SiC, 250 kHz, 3 kg
< 1liter?

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Google's Little Box Challenge; A $1 Million Prize For Creating A Better, **Smaller**, Solar Power Inverter

10.05.2014

Today at an event with President Obama, we announced the Little Box Challenge, a $1 million prize to develop the next generation of power inverters. This prize is one of Google's many efforts to advance a clean energy future. We have a goal of powering our operations with 100% renewable energy, and to that end have contracted over a gigawatt of wind energy for our data centers. Beyond powering our own operations, we've also committed over $1 billion to 16 renewable energy projects around the world. Keep an eye on www.littleboxchallenge.com for more information in the coming months!

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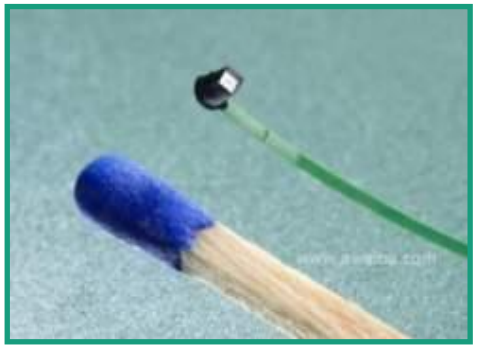
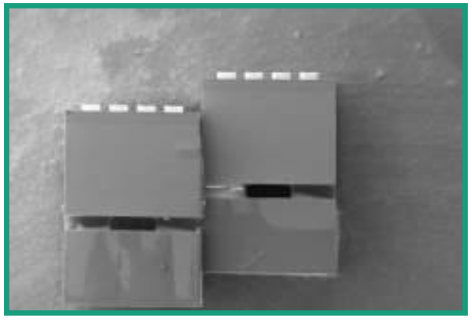
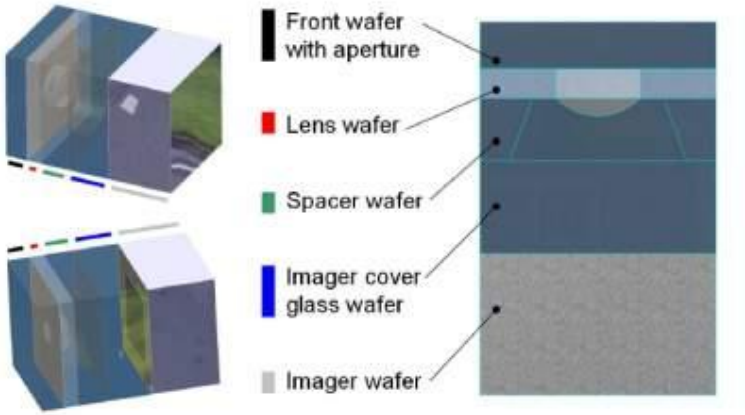
Example: Miniaturized Wafer-Level-Camera



- Wafer level integration of optics and camera electronics
- Module size: 0.7 x 0.7 x 1.0 mm³
- Application: Medical Devices





Courtesy of Awaiba

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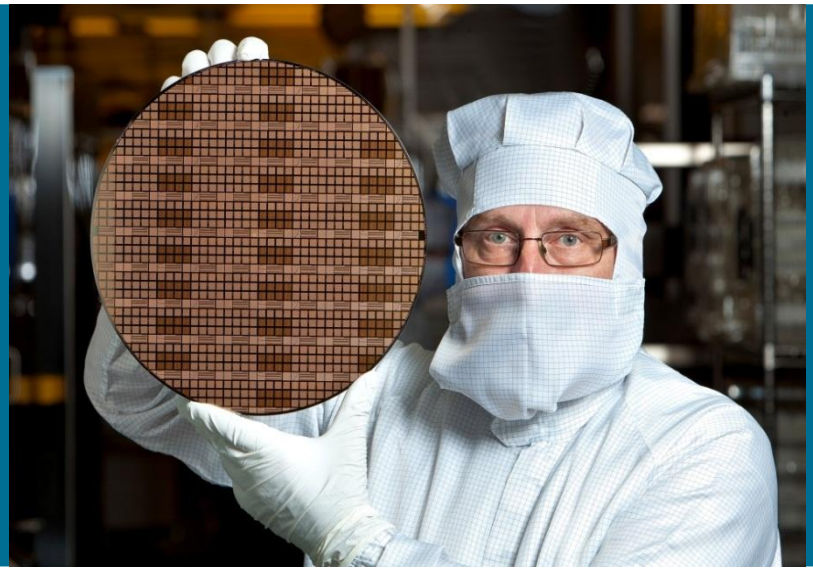
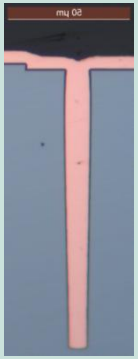
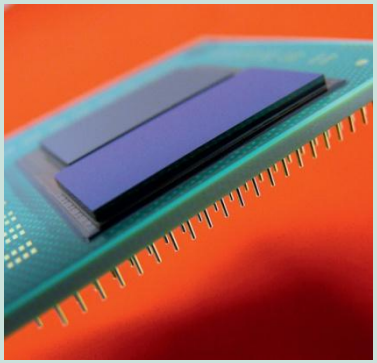
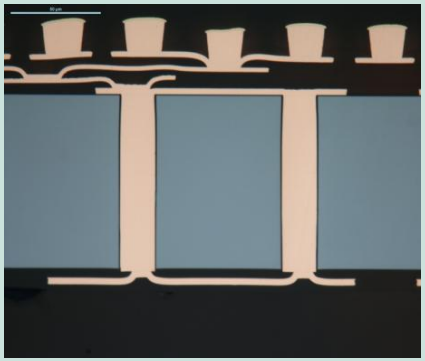
Wafer Level Systemintegration

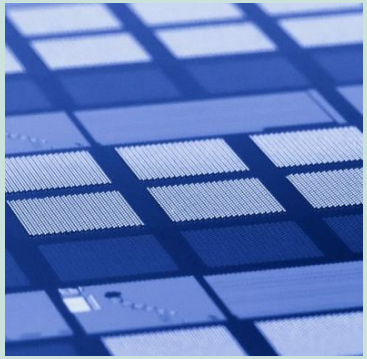
- Thinfilm technologies, Bumping
- Wafer thinning, Thin Wafer Handling
- Through Silicon Via (TSV) Formation
- High density metallization, redistribution
- Interposer, assembly and interconnection technologies











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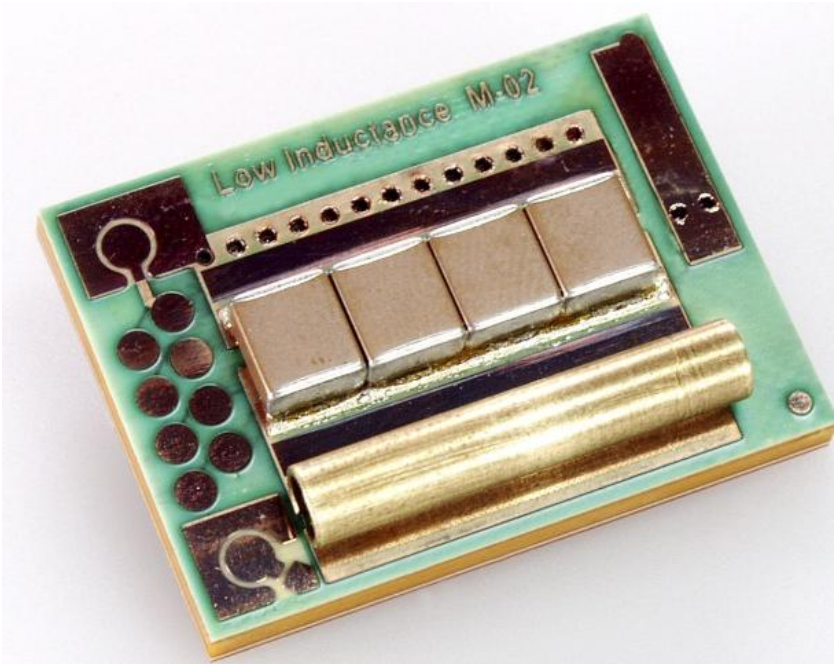
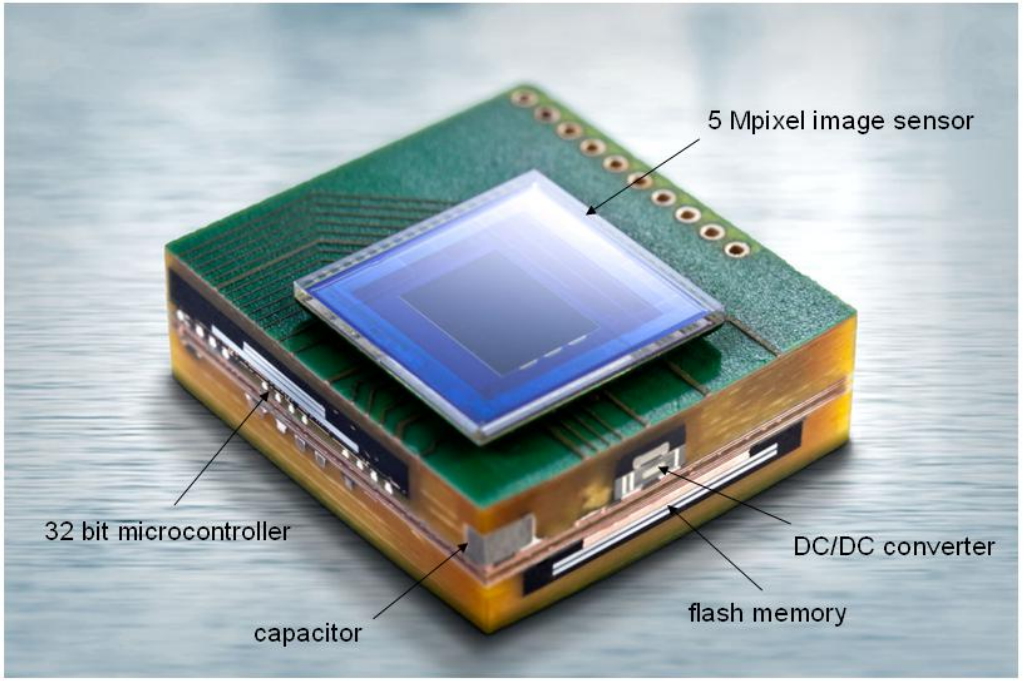
Demonstrators with Embedded Components Manufactured at IZM on Panel Level

Power



Ultra-low inductance power module 600 V / 20 A with DC link inductance below 8 nH (today's world record)

Signal Processing



Modular camera with embedded 32 bit image processor, 2 memory chips, 4 voltage regulators and 72 passives

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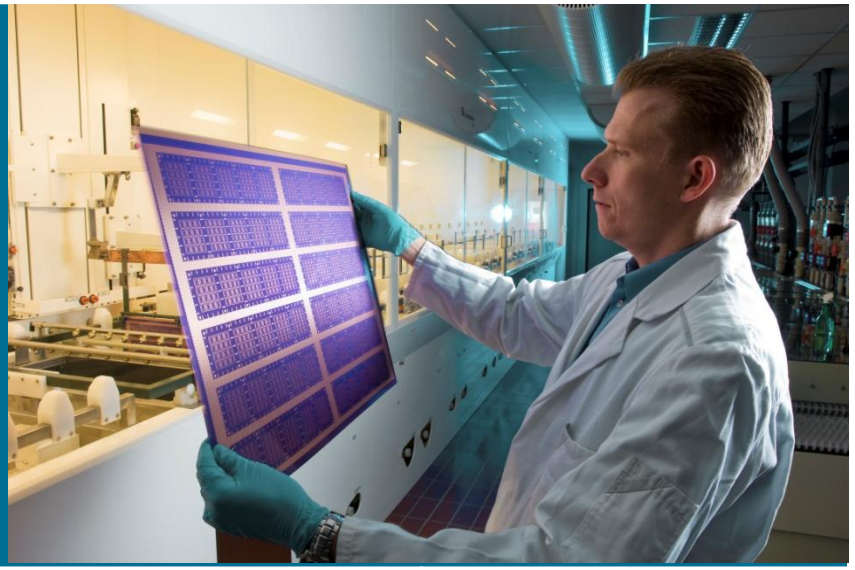
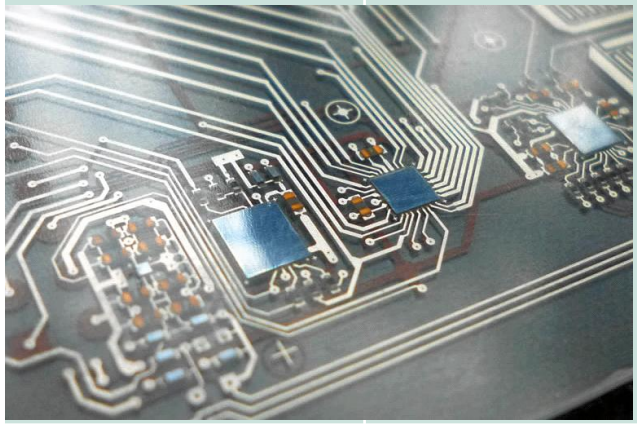
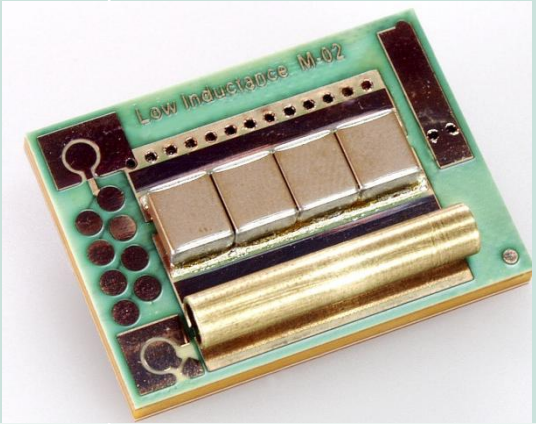
Solutions with polymer substrates

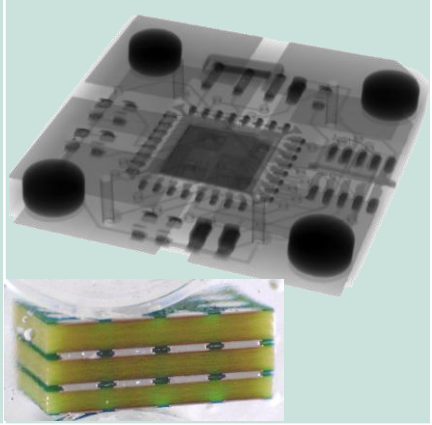
Panel Level Systemintegration

- High density wiring
- High K and low K **dielectrics**
- Thin chip handling and assembly
- Ultra thin interconnects
- Embedded actives and passives
- Functional layer integration









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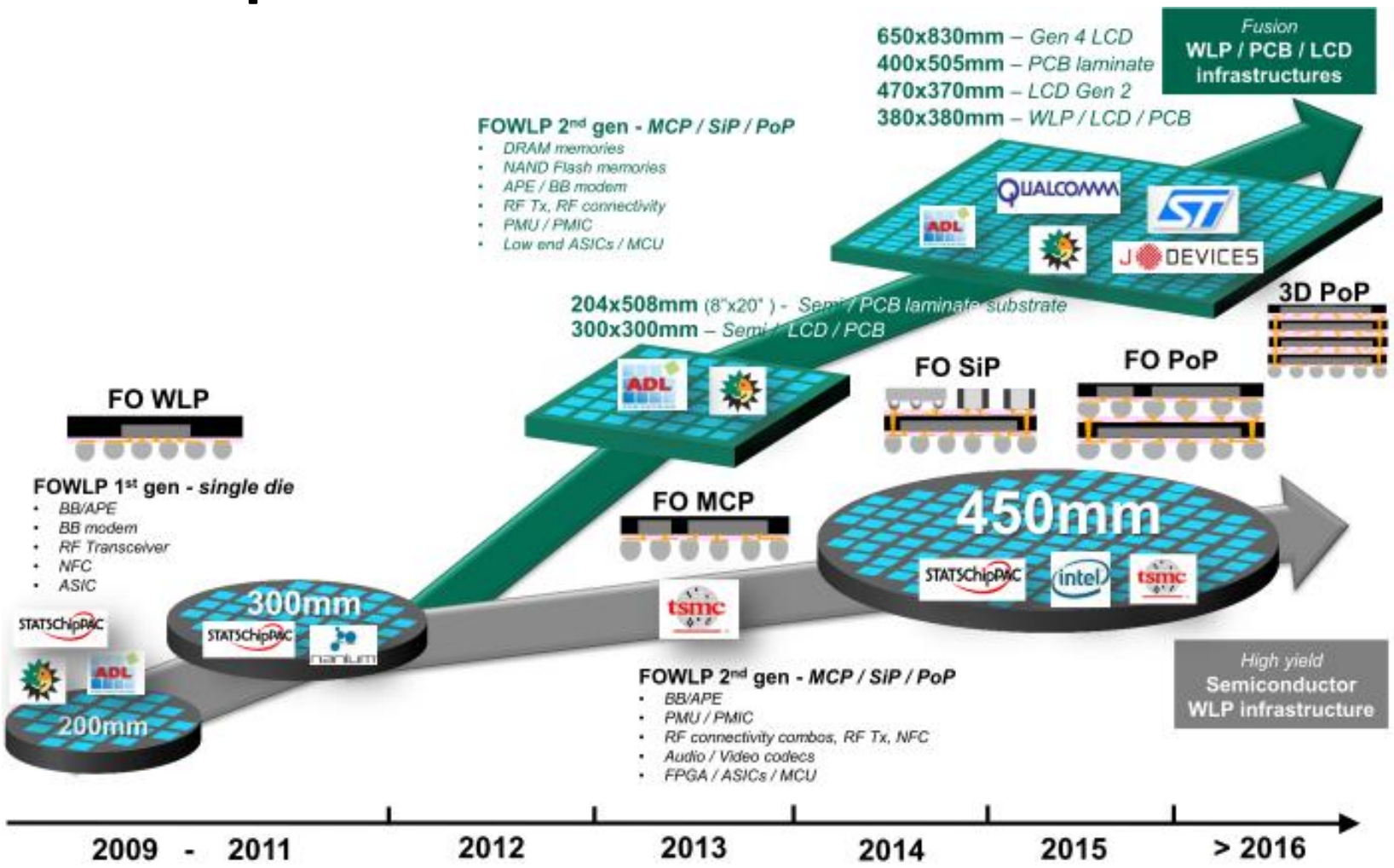
Roadmap Panel Level and Wafer Level



Source: Yole

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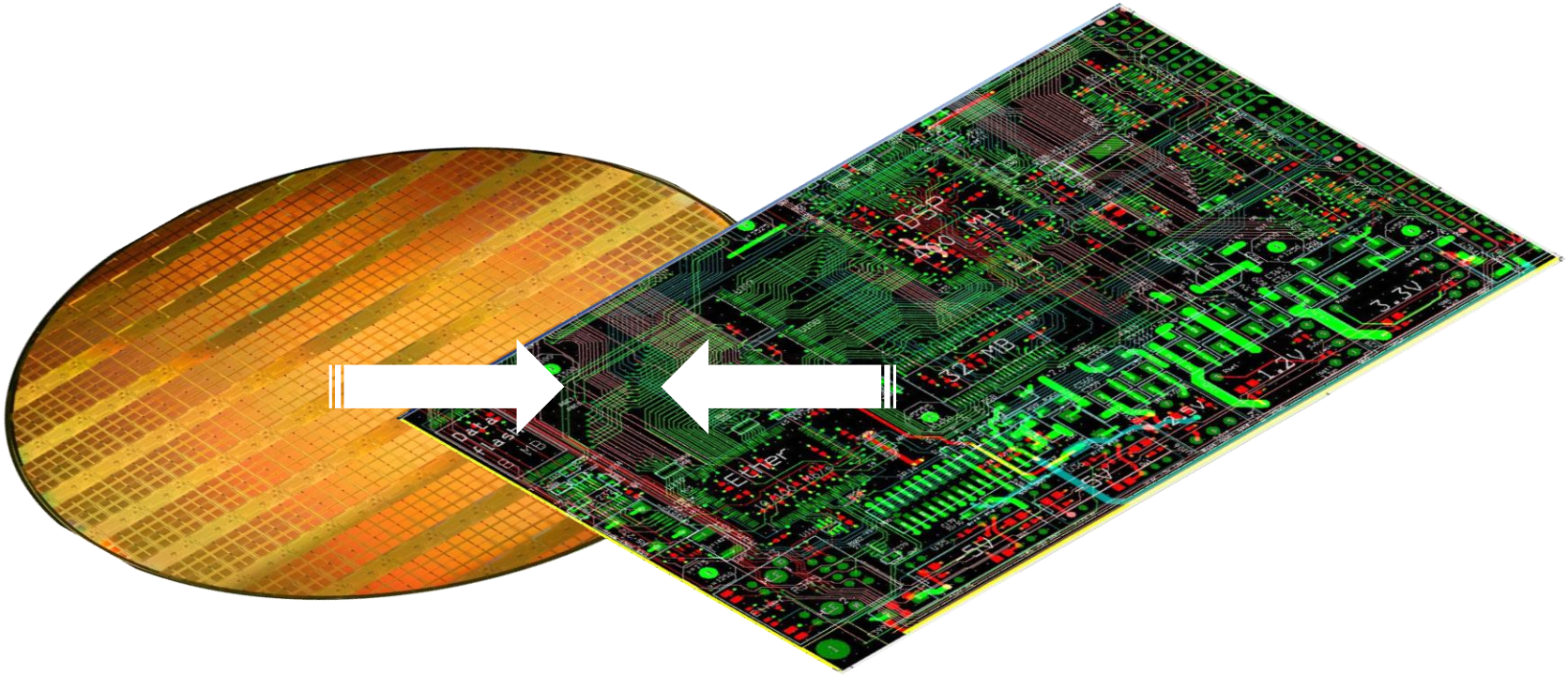
Panel Level is: The intelligent combination of

Wafer Level Processing and Printed Circuit Board Processing



- Finer lines and spaces in combination with semiconductor equipment and organic substrates
- Embedding of bare dies into organic substrates

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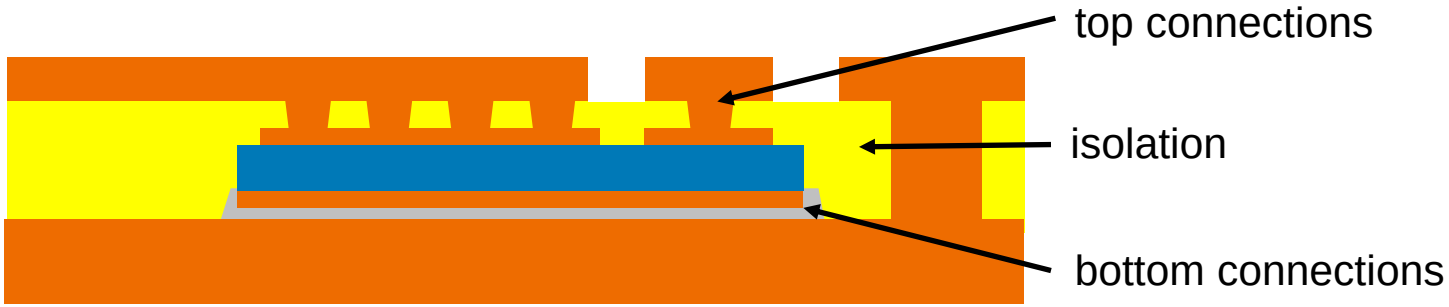
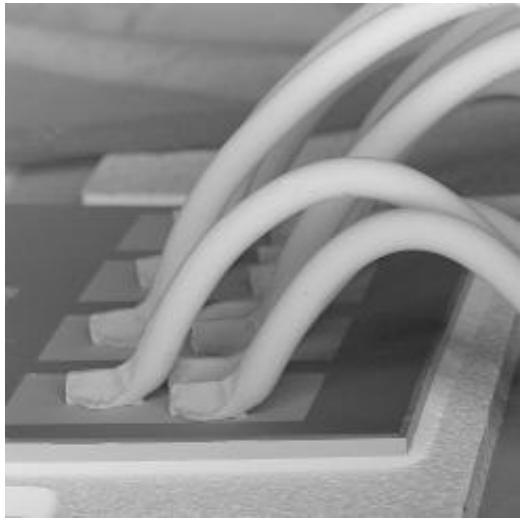
The New DNA for Power Packaging



➔ Integration of components **into** organic substrate structures



Al **wire bonded** IGBT on DCB

replacement of
bond wires

by plated
Cu connections

embedded MOSFET

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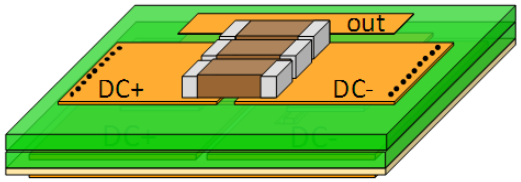
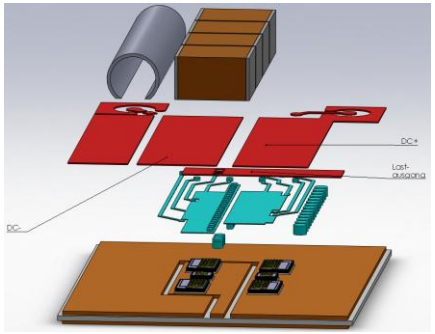
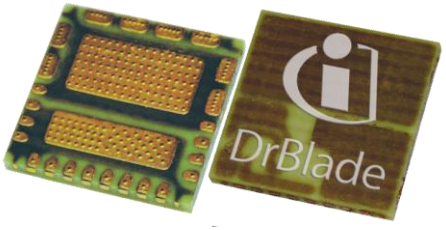
Power Chip Embedding - Opportunities

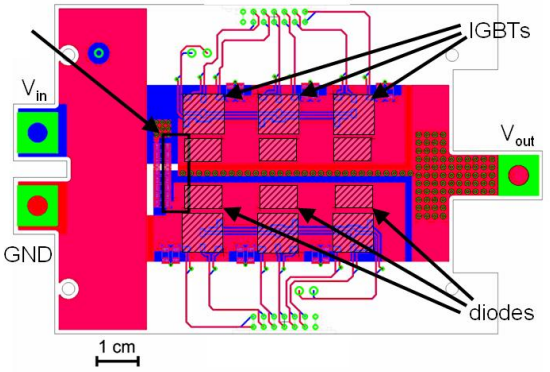
wire bonding on DCB

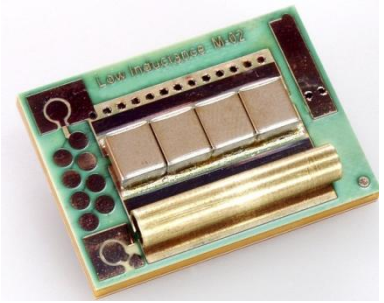
embedding











➔ strong restriction of designs by technological limits

➔ a huge design space is open for exploration

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History and DNA of Fraunhofer IZM!

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DNA of Fraunhofer IZM 2003

2008: Independence of Prof. Geßner's group

Groundbreaking ceremony in Chemnitz

Since that time we established a good cooperation between IZM an ENAS, and many personal relationships have been the result of this cooperation

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Congratulations to the 60th birthday of Prof. Thomas Geßner (Pioneer in Microtechnology)

Staff: Fraunhofer IZM

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